Assignment 2

Remember in all of the problems described here that transmission rates always use the decimal prefixes (e.g., 1K = 1000), whereas storage measurements use binary prefixes (e.g., 1K = 1024).

1. (10%) A computer system contains 1000 identical disk drives, and each of these drives has MTTF of 1,200,000 hours.
   (a) How many drive failures are expected to occur within the first year of operation of this system?
   (b) On average, how many hours will transpire between successive drive failures?

2. (15%) A disk drive manufacturer performs a statistical assessment of the reliability of its disks by putting 6 disks into service and recording the hours of operation and failure during the course of 10,000 hours. They obtain the following data

Drive #	Sequence of up and down time (hours)
1	5000 up, 2 down, 4998 up
2	8000 up, 10 down, 1990 up
3	10000 up
4	2000 up, 2 down, 7000 up, 10 down, 988 up
5	8000 up, 5 down, 1995 up
6	10000 up

   (a) What is the annual failure rate of this collection of disk drives?
   (b) What is the MTTF based on this data?
   (c) What is the MTBF based on this data?

3. (30%) Suppose that a magnetic disk drive has the following parameters:

Number of tracks on a surface	16,384
Number of usable surfaces	1
Number of sectors per track	128
Number of bytes per sector	512
Rotation rate	9600 RPM
Controller overhead per transfer	2.5 ms
Transfer rate	50 MB/sec
Speed of disk head	10 tracks/msec

   (a) What is the total capacity of the disk?
   (b) Given that the average number of tracks traveled in a seek is one-third of the total number of tracks, what is the average time to read a single sector?
   (c) What is the average time to read 16 KB in 32 consecutive sectors in the same cylinder?
   (d) Suppose that sectors are numbered clockwise from 0 to 127, and that tracks are numbered starting with 0 in the outermost track, and the disk rotates counterclockwise (so that sectors are read in increasing order.) To maximize performance, consecutive blocks are stored in the same track if they all fit, and if not, then on the next track in increasing order of track number. Thus, a very large sequence of blocks would be written to track n, then to track n+1, then track n+2, and so on. The head has to be moved over the next track before the data can be read from that track. If more than 128 consecutive blocks are to be stored on the disk to minimize the time to read that sequence, and the first block is stored in track 0, sector 0, in which sector on track 1 should block 128 be placed?

(e) Now suppose we have an array of 4 of these single-surface disks. They are all synchronized such that the arms on all the disks are always on the same sector within the track. The data is striped across the 4 disks so that 4 logically consecutive sectors can be read in parallel. What is the average time to read 128 KB in consecutive sectors from the disk array?

4. (5%) A NAND Flash memory card has a data transfer rate of 50 MB/second. The controller transfer rate is 400 MB/second. What is the average time to read a 2048 byte block?

5. (30%) Suppose that a computer has a 2 GHz clock, and that the instructions in the operating system that are executed to perform polling operations use 800 clock cycles. For each of the following devices, state whether it is possible to use polling to communicat ewith the device, and explain why or why not. If polling can be used, determine the overhead as a percentage, and determine the maximum possible bandwidth.

   (a) A keyboard that can send a packet up to 30 times per second, each containing up to four bytes of data.

   (b) A USB 2.0 external storage device that can transfer 2 bytes at a rate of 60 MB/second.

   (c) A SATA hard disk capable of transfering 32-word blocks at a rate of 80 MB/second.

6. (10%) A computer has a 1 GHz clock. Its hard disk drive uses DMA and can transfer data in 1024 byte blocks at a sustained bandwidth of 24 MB/second. Each transfer requires 600 clock cycles to initiate the I/O and 1400 clock cycles for post-processing in the CPU. If the disk is busy 30% of the time, what is the CPU overhead of the DMA controller?