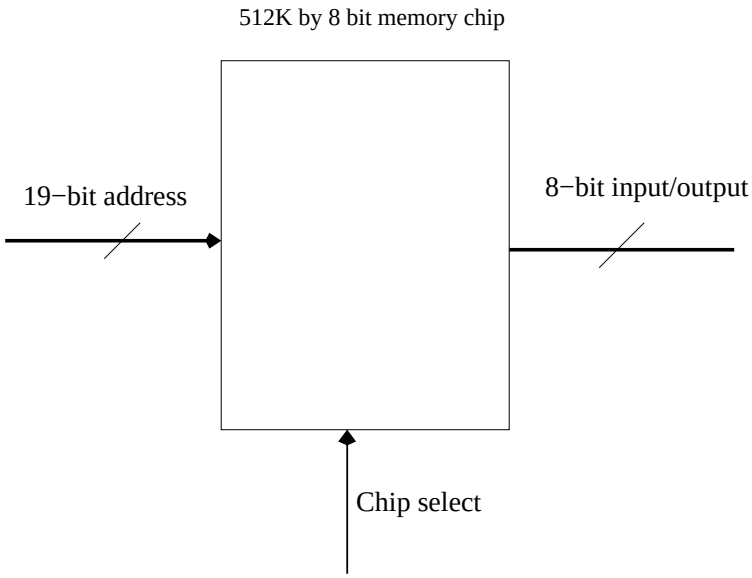
Assignment , Part A

1. (20%) Suppose that you have a supply of 512K x 8 memory chips of the form shown below and you need to construct an 8M x 32 memory. Draw a block diagram like the ones shown in the textbook and in my notes, showing any decoders and/or multiplexors required and how the data and address lines are used and connected to the individual chips and other components. Make the array of chips equal height and width.



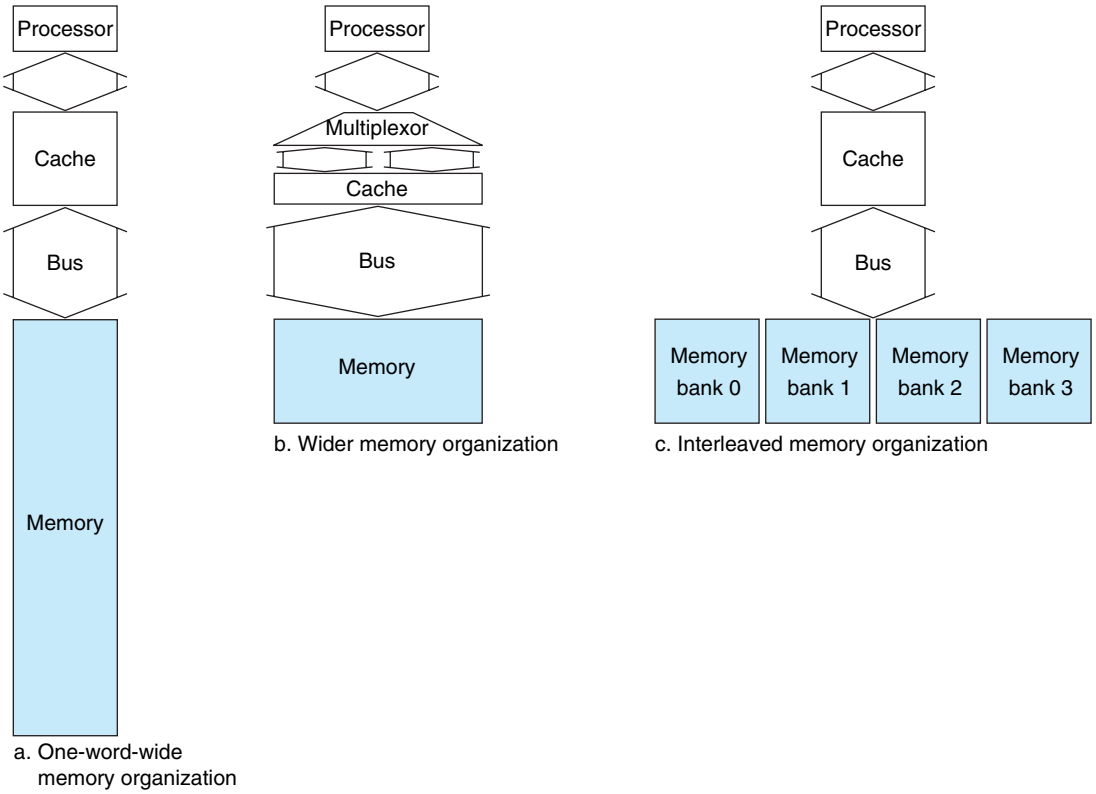
2. (15%) This question has three parts, based on the following sequence of byte addresses generated by the processor:

   4, 80, 136, 208, 200, 220, 132, 320, 332, 220, 4, 80,136, 208, 200, 132

   (a) Given a direct-mapped cache with 16 one-word blocks that is initially empty, label each reference as a hit or a miss and show the final contents of the cache.

   (b) Do the same thing as in part a, except this time assume that the cache has 4 four-word blocks.

   (c) Do the same thing as in part a, except this time assume the cache has 2 eight-word blocks.



3. (15%) Consider the three different organizations of the memory hierarchy shown in Figure 17 of my lecture notes, replicated above. Suppose that the cache block size is 16 words, that the width of the organization in part (b) of the figure is 4 words, and that there are 4 banks in the organization in part (c). If the main memory latency for a new access is 10 cycles and the transfer time is 1 cycle, what are the miss penalties for each of these organizations? Your answer should have three parts labeled (a), (b), and (c).